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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 18

Application Number: 09/216,214
Filing Date: 12/18/98
Appellant(s): Havemann et al.

Jay M. Cantor

For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 04-19-01.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejections of claims 8-10, 12, 14, 16, 18, 20, 22, 24, 26 and 27 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

US 5,841,174	Arai	11-1998
US 4,727,038	Watabe et al.	02-1988
JP 4-42938	Tada	02-1992

(10) Grounds of Rejection

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any

person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The recitation of source/drain regions each disposed adjacent to and aligned with the silicide layer disposed on the sidewalls in claim 10 can be interpreted as setting forth structure not supported by the specification. First of all, Fig. 2D clearly supports a structure immediately after being silicided having the source/drain regions 80 formed not aligned with the silicide layer 60. Secondly, after the formation of the metal silicide layer 60, due to the reaction (movement) between silicon atoms of the polysilicon gate 20 near the gate sidewalls with metal atoms of the metal layer 50 to form the metal silicide layer 60, the boundary between the polysilicon gate 20 and the metal silicide layer (or the gate sidewalls) has shifted. In other words, the boundary or the gate sidewalls have moved inward to the gate center because a portion of the polysilicon gate near the metal layer has been consumed and converted into metal silicide during the annealing (heating) process. Therefore, the location of the gate sidewalls immediately after the silicide layer is formed is unknown and undetermined. Furthermore, the specification also discloses the dispersing of the dopants in step 155 which would make it apparent to one having ordinary skill in the art that the source/drain regions 80 in Fig. 2D would be diffused further under the gate and the boundary of

the source/drain regions 80 with the channel region would also be shifted. As a result, after the formation of the metal silicide layer 60, because of the movement at two locations, at the gate sidewalls and at the source/drain regions in the substrate, source/drain regions 80 are no longer aligned and are not aligned with the silicide layer.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8-10, 12, 14, 16, 18, 20, 22, 24, 26 and 27, insofar as in compliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai (US 5,841,174) in view of Watabe et al. (US 4,727,038).

Arai discloses a transistor gate structure (Figs. 2B, 3A) comprising a gate dielectric 103 over a semiconductor region 101; a patterned gate 104a of polysilicon over said gate dielectric having sidewalls, a top surface and a bottom surface; a lateral growth 110 on the gate dielectric at the corners of the patterned gate, but not under central regions of the patterned gate, a thickness of the gate dielectric continually increasing at the interface of the bottom surface and the sidewalls of the patterned gate in a direction from the bottom surface toward and along the sidewalls (see Fig. 3A); and source/drain regions 107a in said semiconductor region defining a channel under the patterned gate. Arai does not disclose a unitary electrically conductive metallic material of

titanium silicide covering the sidewalls and the top surface of the patterned gate. It is old to form a transistor gate structure comprising a unitary electrically conductive metallic material of titanium silicide covering sidewalls and a top surface of a patterned gate as shown for example by Watabe et al. (layer 60 in Figs. 9A-9E). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the conventional feature (unitary electrically conductive metallic material of titanium silicide) onto the sidewalls and the top surface of the patterned gate 104a of Arai in order to derive a portion of hot carriers through the gate electrode, and therefore the MOS transistor device whose transconductance is not degraded by hot carrier injection is obtained. As a result, the source/drain regions 107a is formed adjacent to the titanium silicide layer disposed on the sidewalls. Also, it flows naturally from the combination of Arai and Watabe et al. references that the titanium silicide layer covering the top and the entire sidewalls of the polysilicon gate 104a would extend to the gate dielectric 103 and the dielectric 106, and the dielectric 106 extends from the gate dielectric 103 of increased thickness relative to the gate dielectric and disposed under the titanium silicide layer.

Arai further discloses a lightly doped source/drain extension (n-- region) of each of said source/drain regions 107a extending under said polysilicon gate 104a.

In the specification, applicant admits that the present invention uses the conventional "smiling" oxidation technique (see page 4, lines 2-11 of the application) to widen the oxide thickness at the corners of the gate that is not different from the oxidation technique used by Arai to form bird's beak on the edge of the gate (see Fig. 3A and col. 6, lines 60-67 and col. 7, lines 1).

Therefore, Arai clearly teaches the same structure using the same oxidation process used by Applicant to inherently form the same feature, a lateral growth on the gate dielectric at the corners of the gate but not under the central regions of the gate. In conclusion, the conventional processing techniques used by Applicant to form a lateral growth on the gate dielectric does not change the resulting product and make it patentable distinguished over Arai's structure.

(11) Response to Argument

On page 4 and page 7 of the appeal brief regarding the rejection of claim 10 under 35 USC 112, first paragraph for claiming source/drain regions aligned with a silicide layer on the sidewalls of the gate as setting forth structure not supported by the disclosure, Appellant argues that the rejection is without merit because the source/drain regions 80 are aligned and must be aligned with the silicide layer 60. According to Appellant, page 8, lines 9-11 of the application and Fig. 2C clearly teach the portion of the substrate under the gate and sidewalls being masked by the metal layer 50 from receiving the implant that form source/drain regions 80. Therefore, the source/drain regions 80 are formed aligned with the silicide layer 60 which is merely the metal layer 50 converted to the silicide layer 60. Appellant concludes that claim 10 and the subject matter are fully set forth in the specification. The examiner respectfully disagrees with the argument. First of all, Fig. 2D of the application clearly shows the source/drain regions 80 are not aligned with the silicide layer 60. Secondly, according to Fig. 2C and page 8, lines 9-11 of the specification, it is true that source/drains 80 are formed aligned with the metal layer 50 before the formation of the metal silicide layer 60. However, after the formation of the metal silicide layer

60, due to the reaction (movement) between silicon atoms of the polysilicon gate 20 near the gate sidewalls with metal atoms of the metal layer 50 to form the metal silicide layer 60, the boundary between the polysilicon gate 20 and the metal silicide layer (or the gate sidewalls) in Fig. 2D no longer remains at the same position as in Fig. 2C. In fact, the boundary or the gate sidewalls have moved inward to the gate center because a portion of the polysilicon gate near the metal layer has been consumed and converted into metal silicide during the annealing (heating) process. Furthermore, the specification also discloses the dispersing of the dopants in step 155 which would make it apparent to one having ordinary skill in the art that the source/drain regions 80 in Fig. 2D would be diffused further under the gate and the boundary of the source/drain regions 80 with the channel region would also be shifted. As a result, after the formation of the metal silicide layer 60, because of the movement at two locations, at the gate sidewalls and at the source/drain regions in the substrate, source/drain regions 80 are no longer aligned and are not aligned with the silicide layer. Appellant errs when stating that merely the metal layer 50 is converted to the silicide 60. It is clear that the metal silicide layer 60 comprises silicon and metal (titanium) and one would wonder where the silicon came from if not from the adjacent patterned polysilicon gate 20. Therefore, a portion of the patterned polysilicon gate 20 and the metal layer 50 must be converted to the silicide layer 60. A careful observation of Fig. 2C and Fig. 2D clearly shows that the silicide layer 60 indeed encroaches and consumes a portion of the patterned gate 20 and the gate sidewalls have moved. The 35 USC 112, first paragraph rejection is valid and maintained.

On page 6 of the appeal brief regarding claims 8-9 rejected under 103(a) as being unpatentable over Arai in view of Watabe, Appellant argues that there is nothing in the combined teachings of the references that would suggest or teach a lateral growth on the gate dielectric. The examiner respectfully disagrees with the remark because it is clear as explained in details above that the modified Arai discloses using the same conventional processing technique to form a bird's beak on the corners of the gate dielectric which inherently form a lateral growth on the corners of the gate dielectric (see Fig. 3A of Arai and Fig. 2D of Application, the corners of the gate dielectrics are not different from each other).

On page 8 of the appeal brief regarding claim 12, Appellant argues that claim 12 requires the silicide layer be titanium silicide and no such arrangement is taught by Arai, Watabe et al. or Tada. The examiner respectfully disagrees with the remark. Watabe clearly teaches a titanium silicide layer 60 covering the patterned polysilicon gate 3 wherein the titanium silicide 60 is formed by siliciding the high melting point metal 55 of titanium (see col. 7, lines 7-17 and Figs. 9C-9E).

On page 8 of the appeal brief regarding claims 14 and 16, Appellant argues claims 14 and 16 require a lightly doped source/drain extension of each of the source/drain regions extending under the polysilicon gate and no such arrangement is taught by Arai, Watabe et al. or Tada. The examiner respectfully disagrees with the remark. Fig. 3A of Arai clearly discloses a lightly doped source/drain extension (n--) of each of the source/drain regions 107a extending under the polysilicon gate 104a.

On page 8 of the appeal brief regarding claims 18, 20, 22 and 24, Appellant argues these claims require a dielectric extending from the gate dielectric of increased thickness relative to the gate dielectric and disposed under the silicide layer and no such arrangement is taught by Arai, Watabe et al. or Tada. The examiner respectfully disagrees with the remark. The modified Arai's structure would provide the dielectric 106 extending from the gate dielectric 103 and disposed under the silicide layer. It flows naturally from the combine. Arai in Fig. 3A clearly shows a dielectric 106 extending from the gate dielectric 103 of increased thickness relative to the gate dielectric 103. Arai does not teach a silicide layer covering the patterned polysilicon gate 104a and the dielectric 106 disposed under the silicide layer. Watabe et al. teaches the use of titanium silicide layer covering a patterned gate to prevent the degradation of the device caused by hot carrier injection. As a result, the combination of Arai and Watabe et al. would provide a unitary titanium silicide layer covering the polysilicon gate 104a of Arai wherein the dielectric 106 (see Fig. 3A) would be formed under the silicide layer.

On page 8 of the appeal brief regarding claim 26, Appellant argues this claim requires the silicide layer extend to the gate dielectric and no such arrangement is taught by Arai, Watabe et al. or Tada. The examiner respectfully disagrees with the remark. The modified Arai's structure would provide the silicide layer covering the entire sidewalls of the patterned gate 104a extending to the gate dielectric 103. It flows naturally from the combine. Arai in Fig. 3A shows the gate dielectric 103 formed under the patterned gate 104a. Arai does not teach a silicide layer covering the entire sidewalls of the patterned polysilicon gate 104a. Watabe et al. teaches the use of

titanium silicide layer covering the entire sidewalls of a patterned gate to prevent the degradation of the device caused by hot carrier injection. As a result, the combination of Arai and Watabe et al. would provide a unitary titanium silicide layer covering the entire sidewalls of the polysilicon gate 104a of Arai wherein the silicide layer would extend to the gate dielectric 103.

On page 9 of the appeal brief regarding claim 27, Appellant argues this claim requires the silicide layer extend to the dielectric and no such arrangement is taught by Arai, Watabe et al. or Tada. The examiner respectfully disagrees with the remark. The modified Arai's structure would provide the silicide layer covering the entire sidewalls of the patterned gate 104a extending to the dielectric 106. It flows naturally from the combine. Arai in Fig. 3A shows the dielectric 106 being adjacent the gate dielectric 103 under the patterned gate 104a. Arai does not teach a silicide layer covering the entire sidewalls of the patterned polysilicon gate 104a. Watabe et al. teaches the use of titanium silicide layer covering the entire sidewalls of a patterned gate to prevent the degradation of the device caused by hot carrier injection. As a result, the combination of Arai and Watabe et al. would provide a unitary titanium silicide layer covering the entire sidewalls of the polysilicon gate 104a of Arai wherein the silicide layer would extend to the dielectric 106.

In conclusion, it is respectfully submitted that a prima facie case of obviousness has been established and that Appellant has failed to rebut.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

tt

August 9, 2001

The conferee of appeal conference: Thien Tran TT

conference was held on July 10, 2001

Tom Thomas T.T

Charles Bowers CLB